In the Claims:

Claims 1-54 (Canceled).

55. (Original) A content addressable memory (CAM) device, comprising:

a CAM array block having at least one row therein that comprises a plurality of CAM cells and a dual-function check bit cell pair that is configurable as a CAM cell when necessary to account for a defective CAM cell in the at least one row.

56. (Original) The CAM device of Claim 55, wherein the at least one row comprises a plurality of dedicated check bit cells that are not configurable as CAM cells.

57. (Original) The CAM device of Claim 56, wherein at least some of the dedicated check bit cells are configured to retain parity data.

58. (Currently amended) The CAM device of Claim 56, wherein a first dedicated check bit cell in the plurality thereof is configured to be less susceptible to soft errors relative to a check bit cell in the dual-function check bit cell pair by virtue of the fact that latching inverters within the first dedicated check bit cell are larger than latching inverters within the check bit cell in the dual-function check bit cell pair.

59. (Original) The CAM device of Claim 56, wherein the at least one row comprises at least one redundant check bit cell.

60. (Original) The CAM device of Claim 55, wherein each of the plurality of CAM cells comprises at least one SRAM memory cell having a first pair of inverters therein that define a first latch; wherein the at least one row comprises a dedicated SRAM check bit cell having a second pair of inverters therein that define a second latch; and wherein the second pair of inverters are larger than the first pair of inverters.

Claims 61-76 (Canceled).

77. (New) The CAM device of Claim 55, wherein the at least one row further comprises at least one dedicated check bit cell and at least one flag cell therein, said at least one flag cell configured to designate a valid of invalid status of a respective check bit(s) retained by the at least one dedicated check bit cell.

78. (New) The CAM device of Claim 55, wherein the dual-function check bit cell pair comprises a 4T compare circuit.

79. (New) The CAM device of Claim 55, wherein the CAM cells are static CAM cells.

80. (New) The CAM device of Claim 55, wherein the plurality of CAM cells and the dual-function check bit cell pair are electrically connected to a match line associated with the at least one row.

81. (New) The CAM device of Claim 80, wherein the at least one row comprises at least one dedicated check bit cell that is not electrically connected to the match line.

82. (New) The CAM device of Claim 56, wherein a first dedicated check bit cell in the plurality thereof is configured to be less susceptible to soft errors relative to a check bit cell in the dual-function check bit cell.

83. (New) A content addressable memory (CAM) device, comprising:

a CAM array block having a row therein comprising a plurality of CAM cells, a plurality of dedicated check bit cells and a dual-function check bit cell pair that is configurable as a CAM cell when necessary to account for a defective CAM cell in the row.

84. (New) The CAM device of Claim 83, wherein the row further comprises a redundant check bit cell therein.